REMARKS

In response to the Final Office Action mailed June 20, 2002, reconsideration is respectfully requested in view of the following remarks. To further the prosecution of this application, Applicants have addressed each of the issues raised in the Office Action, as discussed below.

Claims 1-9, 11, 16-24, 27, 29, and 31-40 are now pending in this application, of which claims 1, 4, 7, 11, 16, 22, 27, 29, 30, and 33 are independent claims. In this response, no claims have been amended. The application as now presented is believed to be in allowable condition.

A. Preliminary Matters

Applicants point out that the Office Action, in detailing the disposition of claims, has listed claim 11 as having been withdrawn from consideration. Applicants withdrew claim 10, 12-14, both claims numbered 15, 25, 26, and 31 in a mailing dated August 13, 2001, in response to the Office Action mailed on July 12, 2001. Claim 11 has not been withdrawn from consideration, and is still pending. Please see Applicants' Response filed May 3, 2002, wherein it was noted that the Examiner had agreed to include claim 11 in the Group II claims. In addition, claim 41 has not been listed as pending. Claim 41 was added in the Amendment dated May 3, 2002 and has apparently been overlooked.

B. Telephone Conference with the Examiner

Applicants' representative appreciates the courtesies extended by Examiner Phan in granting and conducting a telephone conference on December 2, 2002. During the conference, Applicants' representative requested the Examiner withdraw the finality of the pending Office Action. Applicants' representative noted that the Office Action contained new rejections not necessitated by the previous amendment. For example, the previous amendment to claim 1 did not alter its scope and the new rejections of claim 1 under §§ 112 and 103 equally could have been made against the previous version of the claim. The same is true for a number of other rejections. The Examiner indicated that if a response did not put all claims in condition for allowance, he would withdraw the finality upon receipt of Applicants' response and would give the response full consideration, not imposing the limitations of finality.

C. Objections to the Drawings

In paragraph 1, the Office Action objected to the drawing because they failed to show various elements. Applicants respectfully address each one of the alleged omissions below.

The Office Action states that the drawings fail to show the mixer 72 discussed on line 5, of page 10. The reference numeral of the mixer should have been 74, which is clearly shown in Figure 1. The specification has been amended herein to correct this typographical error.

The Office Action states that the inverter 174, discussed on line 17 of page 12, is not shown. Applicants have amended Fig. 5 to indicate inverter 174, which was incorrectly labeled with reference character 176. Fig. 5 is now believed to be correct.

Further in relation to Fig. 5, the Office Action states that the reference voltage Vref, discussed on line 26 of page 13, is not shown. Additionally, the Office Action states that the references voltages V2, V4, V6, V8 are not shown connected to ground, as discussed on the same line. Applicants respectfully point out that line 26 of page 13 merely discloses a particular possible group of connections according to one embodiment of the invention. It is well known in the art that any number of reference voltages could be used for connection to the reference voltage terminals shown in Fig. 5. Fig. 5 reflects this well known generality and as such is correct. Therefore, Applicants respectfully request that this objection be withdrawn.

The Office Action states that the switches 148, 149, and 150, discussed on line 18 of page 20, are not shown. The reference numerals of the switches in that line of the specification were incorrect due to a typographical error, and the specification has been amended herein to correct the error.

The Office Action states that the non-overlapping four-phase clock discussed on line 9 of page 27 is not shown in the drawings. The four-phase clock is not specifically shown in Fig. 27 and was not intended to be shown, since the use of multiple phase clocks is well known in the art. However, the operation of each of the switches in Fig. 27 is discussed in detail with respect to the four phases of the clock from line 16 of page 27 to line 9 of page 28. Applicants respectfully assert that Fig. 27, in conjunction with the specification, provides adequate structural detail for a proper understanding of the disclosed invention. As such, Applicants respectfully request that this objection be withdrawn.

The Office Action further states that the output of the input op amp discussed on line 16 of page 27 is not shown. Applicants respectfully disagree. Fig. 27 clearly shows the inputs and output of each op amp in the figure. The operation of op amps and their symbolic representation in schematics is well known in the art; thus, Applicants believe that the op amps and their respective inputs and outputs as shown are enough to provide adequate structural detail for a proper understanding of this invention. Accordingly, Applicants request that this objection be withdrawn.

Finally, the Office Action states that the latch stage 804, as described on line 17 of page 33, is not shown. Fig. 25 has been amended to label the latch stage with the reference character 804. The description of Fig. 35 in the specification was correct, and Fig. 35 is now in agreement with the specification. Applicants therefore request that this objection to the drawings be withdrawn.

D. Rejections Under 35 U.S.C. §112, First Paragraph

Claims 1-9, 16-24, 27-29, and 31-40 were rejected under 35 U.S.C. §112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Applicants respectfully traverse these rejections.

The Office Action states at paragraph 2, page 3 that:

> "the specification does not describe the following features: the mixer circuit in Fig. 2; the QDAC1 to QDACN and the charge sharing network in Fig. 4; the elements 176 and P1 + P2 in Fig. 5; Fig. 6; the master clock and signal P4 in Fig. 9; the switch connecter between element 164 and S19 in Fig. 10; all elements in Figs. 28A-B; all the switches, capacitors and elements from SCF, selectable gain, External CAP and Voltage output in Fig. 30; and elements P1 + bit1.P2, P1 + bit2.P2, P1 + bit3.P2 and P1 + bit4.P2 in Fig. 31."

As previously discussed, the discussion of the mixer 74 in Fig. 1 and Fig. 2 was erroneously labeled by reference character 72 in the specification. This typographical error has been corrected herein. The mixer of Fig. 1, which is discussed on line 5 of page 10, is the same mixer shown in Fig. 2. Furthermore, it is respectfully asserted that mixer circuits are well known to those skilled in the art. Therefore, Applicants respectfully assert that the mixer circuit of Fig.

2 has been described in such a way as to enable one of ordinary skill in the art to make or use the invention.

Fig. 4, which merely serves as an illustrative block diagram, is described on page 11, line 24 to page 12, line 2. As discussed in the specification, the block diagram of Fig. 4 demonstrates the manner in which the multi-bit digital input is related to the analog output. Namely, the analog outputs QDAC1 through QDACN of the block diagram show signals which are indicative of a sum of values in the multi-bit signal. The purpose of this figure was merely to demonstrate generically some possible relationships between the digital inputs and the analog outputs, which are discussed later in more detail, along with the charge sharing network. Therefore, it is believed that the specification does, in fact, describe Fig. 4.

The Office Action states that the specification does not describe the elements 176 and P1 and P2 of Fig. 5 in the specification. Applicants disagree. As discussed earlier, the reference character of the inverter element 174 was incorrect in the originally filed Fig. 5, and has been corrected herein. In addition, the true element 176, which is properly labeled in Fig. 5 at the output of inverter 174, is discussed in the specification at page 12, line 17. Control signals P1 and P2 are also described in the specification in relation to Figs. 5 and 6, from page 13, line 27 to page 14, line 8.

The Office Action states that Fig. 6 is not described in the specification. As previously noted, the paragraph beginning at line 27 of page 13, which obviously describes Fig. 6 but mistakenly referenced Fig. 3, has been amended. The description of Fig. 6 should now be clear.

The master clock and signal P4 are described in the specification at page 16, lines 9-13 and 15-16.

The Office Action further states that the switch connected between element 164 and S19 in Fig. 10 is not described in the specification. Applicants have amended the drawings herein to correct the inadvertent omission of the reference character S14 labeling the switch between elements 164 and S19 in Fig. 10. This labeling is clearly consistent with rest of the figure and has clear support in the specification at page 17, lines 15-16 of the specification.

Contrary to the assertion on page 3 of the Office Action, full support for all the elements of Figs. 28A-B is clearly given in the specification from page 29, line 27 to page30, line 16.

The Office Action additionally states that the specification does not describe: "all the switches, capacitors and elements from SCF, selectable gain, External CAP and Voltage output

in Fig.30." The elements of Fig. 30 are described in the specification from page 30, line 31 to page 31, line 7. Fig. 30 is merely meant to provide an illustrative embodiment of the CT filter 92 shown in Fig. 2, and as such, is not described in great detail. However, Fig. 30 is fully described by the specification to the extent necessary to provide an exemplary embodiment of an element of the invention to those skilled in the art.

The Office Action also states that the elements P1 + bit_1·P2, P1 + bit_2·P2, P1 + bit_3 ·P2 and P1 + bit_4·P2 in Fig. 31 are not described adequately in the specification. Applicants disagree, and respectfully point out that Figures 33A-33C and 34A-34C, along with the relevant portions of the specification (page 31, line 30 to page 33, line 5) explicitly show the relationship between the control signals input to the various switches of the squaring circuit in Figure 31 and the various clock phases P1-P3 and input bits bit_1-bit_4.

Additionally, the Office Action states that none of the equations in Figs. 7A-C, 8A-D, 12A-C, 14A-C, 19A-C, 33A-C, and 34A-C are clearly understood "since Vref and Q(C1), Q(C2), Q(C3), and Q(C4) are not described in the specification." First, Applicants respectfully point out that it may be assumed that one skilled in any electrical art is familiar with the fact that the charge induced on a capacitor is equal to the capacitance of the capacitor times the voltage across the capacitor. This cannot be disputed. Consequently, using perfectly conventional notation, those skilled in the art will know that Q(C1) represents the charge (Q) on a capacitor C1, etc. Secondly, Applicants point out that in the specification, reference is made to the fact the V1, V2, etc., which are stated in the specification to be the inputs to the switched capacitor DACs such as those shown in Figs. 5, 13, 16, 27, etc., may each be connected to unique input voltages, or may all be connected to a common voltage level Vref. An example of this explanation can be found at page13, lines 16-26. As is known to those of ordinary skill in the art, a standard logic level, such as Vref, may be used to represent a logical 1 or 0 in a digital computing environment. In that way, the same voltage Vref may be present on two bit lines even though one bit line represents a value an order of magnitude higher than the other. For instance, a higher-valued bit line may be coupled to a capacitor with a capacitance which is scaled in relation to the value that the bit line represents. Applicant respectfully asserts that facts discussed above, which are certainly known to those skilled in the art, coupled with the teachings of Applicant's specification, more than constitute support for the rejected claims and that the Office Action does not demonstrate to the contrary.

The Office Action further states in its rejection that the switching ON/OFF operation of all the switches in each of Figs. 11-A-D, 15, 16A-E, 17-18, 19A-C, 20-22, 25, 27 and 30 is not understood since no switching control signal is shown in the drawings and is described in the specification. Applicants strongly disagree. For each figure, the discussion of that figure in the specification gives detailed information about the timing and control of the various switches in the figure with respect to the phase signals P1-P4, when applicable. In some cases, for instance in Fig. 15, switches whose timing and control information is not discussed are explicitly stated to serve purposes other than switching. In the case of Fig. 15, these switches serve to balance parasitic effects which could harm performance. Respectively, for Figs. 11, 16-22, 25, 27, and 30, such discussions may be found from page 17, line 22 to page 18, line 19; from page 20, line 26, to page 21, line 16; page 23, lines 1-9; page 23, lines 10-19; page 23, line 20 to page 24, line 4; page 24, lines 18-29 (for Figs. 20, 21, 22, and 25); and page 27, line 16 to page 28, line 9. Thus, Applicants respectfully assert that the switching operations of each of the figures in the specification are fully supported and that no additional drawing figure is needed.

The Office Action also asserts that the connection of elements 202, 204, 206, 208, S49, and S50 in Fig. 15 is not described in the specification. Applicants respectfully disagree. The Examiner is respectfully requested to refer to page 20, lines 16-25 and Figs. 16A-16E of the specification, where the use of the switches in compensating for parasitic effects is discussed, and the layout and connection of the various switches is developed. It can be seen in Fig. 16E that some connections for the switches require more than one SC cell and thus were not identified in Fig. 15.

Likewise, elements S43 and S48 in Fig. 16A-E, whose connections the Office Action asserts are not completely described, depend on being joined with other SC cells (for example in a "ring cell"), and thus by necessity not every single connection can or need be shown in the figure.

The Office Action states that it is unclear how terminals 312 and 314 in Figs. 16B-E are interconnected with each other. As discussed on page 21, line 24 to page 22, line 20, either connection 312 or 314 is needed to connect to an adjacent SC cell, depending on the relative orientation of the two SC cells. Thus, the specification provides clear explanatory language and support.

The Office Action states that elements NC, NAND gates, inverters, switches, capacitors and terminals in Figs. 17, 21-22, and 25 are not described as well as numbered. However, in the context of the previously demonstrated embodiments, these figures are meant to show physical orientations in which the SC cells may be grouped, and as such do not require extensive use of reference characters to label deeper structures. The figures as presented are consistent with both their description in the specification and their intended purpose, and clearly have support.

The Office Action states that "the four arrows on the right side of scrambler 400 are not described as well as numbered." Applicants respectfully assert that scramblers are well known to those skilled in the art of digital to analog conversion, and that figure 24 in conjunction with page 25, lines 10-28 is easily understood by any such person.

Finally, the Office Action states that the feature "an analog signal that is indicative of the multi-bit digital input signal received by the switched capacitor DAC using less than all of the redistributed charge" as recited in the last three lines of claim 29 is not described in the specification. Applicants strongly disagree. Any of Figs. 7A-C, 8A-D, 10, 11A-11D, 12A-C, or 14A-C, in conjunction with their respective descriptions in the specification, show switch timings according to the present invention which result in the production of an analog signal proportional to the digital input which uses less than all of the redistributed charge from the subDACs. For example, Figs. 8A-8D step through one exemplary switching order in which the final charge produced, while being proportional to the digital input, uses only one quarter of the redistributed charge (page 16, line 11 to page 17, line 5). In another example, Figs. 11A-11D demonstrate a DAC and a switch controlling scheme in which an analog charge proportional to the digital input is produced using only one fourth of the redistributed charge, and in which identical copies of the charge are produced which could be used advantageously (page 17, line 22 to page 18, line19). Thus, Applicants assert that ample support is found in multiple places in the specification for claim 29 of the application.

E. Rejections Under 35 U.S.C. §103

1. Claims 1-9 and 34-37 are patentable.

Paragraph 5 of the Office Action rejects claims 1-9 and 34-37 under 35 U.S.C. 103(a) as unpatentable over Fling et al., 4,591,832, in view of Mehta et al., 4,205,203, Lee et al., 6,130,633, and Dingwall et. al., 5,332,997. (It is noted that although claim 34 is listed as being

rejected under 35 U.S.C. 103(a), this is believed to be a mistake since claim 34 depends from claim 33, which has been rejected under 35 U.S.C. 102 over Watson. Therefore, claim 34 is addressed later in conjunction with the rejection of claim 33.) Applicants respectfully traverse these rejections.

a. The Combination is Improper

First, no motivation is provided in the Office Action from the prior art (whether the cited references or otherwise) to make the proposed combination. In order to establish a *prima facie* case of obviousness, their must be some suggestion or motivation in the prior art to make the proposed combination. The Examiner appears to be using the Applicants' own specification as the motivation for the proposed combination; such a use of hindsight is improper. The Office Action has provided no motivation for the proposed combination in either Fling or Mehta or any other references; nor does one exist. Fling is directed to a system for processing the video information in a video signal (col. 1, lines 10-26). In order to enhance the image quality of certain digital video receivers, Fling attempts to double the number of horizontal lines displayed per frame while keeping the frame rate constant (col. 1, lines 27-35). This is because a television rasters the image onto the screen many times a second. Thus, video data is inherently serial; there is no need for a multi-bit DAC in the device of Fling, because Fling attempts to solve a problem which is inherently single bit. Not only would those skilled in the art have perceived no motivation to make the combination, but also it makes no sense to combine the multi-bit signal of Mehta with the device of Fling along with other references. Therefore, the rejection under 35 U.S.C. 103(a) over the combination of Fling and Mehta where the use of a multi-bit signal would be inappropriate to Fling's intended use is improper and should be withdrawn. A break in the first link of a proposed combination destroys the whole chain of combination.

b. Applicants' Claims Distinguish Over the Proposed Combination

Even assuming *arguendo* that the proposed combination of Fling, Mehta, etc. did make sense and further assuming there was some hypothetical motivation, the proposed combination would still not meet and make obvious claims 1-9 and 34-37of the present invention.

If one were to combine the teachings of Fling and Mehta, without reaching the tertiary references, one can posit that the resulting device would use the ping-pong DACs of Fling and

the multi-bit digital input of Mehta, as suggested on page 5 of the Office Action. Each bit of the multi-bit signal would enter a pair of pin-ponged DACs and would be converted to an analog signal at twice the rate as would be accomplished with only one of the DACs. However, such a device would neither anticipate nor make obvious any of claims 1-9 or 34-37, because, contrary to the assertion of the Office Action, Fling does not disclose a system having a DAC that receives a multi-bit digital signal and outputs *at least two* analog signals including a first analog signal and a second analog signal, the first analog signal being indicative of a sum of values of bits in the multi-bit digital signal, the second analog signal also being indicative of said sum of values of the *same bits* in the multi-bit digital signal.

Firstly, Fling discloses only a DAC system having inside it **two DACs** (elements 16 and 18), **each of which output a *single* analog signal** (col. 2, lines 49-58). In contrast, claim 1 recites a system having **a DAC (i.e., a single DAC, not two) that receives a multi-bit digital signal and outputs at least *two* analog signals (i.e., one DAC, two output signals).** Secondly, those output signals include a first analog signal and a second analog signal, the first analog signal being indicative of a sum of values of bits in the multi-bit digital signal and the second analog signal also being indicative of *the same* sum of values of said bits in the multi-bit digital signal. By contrast, each of Fling's ping-ponged DACs operate on *different* input bits and produces a *single* output. Neither of the DACs making up the DAC converter system of Fling, even when modified by Mehta to take in a multi-bit signal, outputs at least two analog signals, with or without the other two references, much less the claimed signals. Therefore, claim 1 is unobvious and patentably distinguishes over the combination of Fling and Mehta, and Applicants respectfully request that the rejection of claims 1-9 and 34-37 be withdrawn.

In addition, thirdly, nowhere in Fling or Mehta is it taught or suggested that the single analog value output by each of DACs 18 and 16 is indicative of a sum of bits. To the contrary, Fling shows, in Figs. 1 and 2, that the output of each DAC is a sample of *every other* value x_n, where x_n is the value of the single bit signal x at time n. In other words, DAC 16 outputs a series of values x_{n-2}, x_n, x_{n+2}, etc., while DAC 18 outputs a series of values x_{n-3}, x_{n-1}, x_{n+1}, etc. In no way do *each* of DACs 18 and 16 of Fling output **two** analog signals **which are indicative of a sum of bits**. Even the output 25 of the sum of the signals 20 and 22 is not indicative of a sum of bits; instead, it is indicative of an analog version of the time-varying single-bit signal 10. Signals

20 and 22 are out-of-phase samples of the same, single-bit signal which combine to produce not two summed signals, but an analog version of the original signal.

Ignoring the fact that there is no demonstrated motivation to combine the pin-pong video converting DACs of Fling with the multi-bit sound signals of Mehta, if one of ordinary skill in the art were asked to combine the two by using one of Fling's one-bit ping-pong DAC systems for each bit of the multi-bit system, such a system would still not meet the claims of the present invention because 1) there would be no DAC that could output two analog signals, and 2) there would be no DAC which could output two analog signal indicative of a sum of values of bits, since each pin-pong DAC pair takes in a single-bit signal.

In contrast, claim 4, the second independent claim, recites a method comprising receiving a multi-bit digital signal and generating at least two analog signals including a first analog signal that is indicative of a sum of values of bits in the multi-bit digital signal, and a second analog signal that is indicative of ***said*** sum of values of said bits in the multi-bit digital signal.

As discussed above, nowhere in Fling or Mehta, or the other references, is it disclosed to generate at least two analog signals including a first analog signal that is indicative of a sum of values of bits in the multi-bit digital signal, and a second analog signal that is indicative of the same sum of values of the same bits in the multi-bit digital signal.

Similarly, claim 7 recites a system comprising means for receiving a multi-bit digital signal and means for generating at least two analog signals including a first analog signal that is indicative of a sum of values of bits in the multi-bit digital signal, and a second analog signal that is indicative of said sum of values of said bits in the multi-bit digital signal.

Thus, for the reasons cited above, claims 1-9 and 34-37 patentably distinguish over, and are not obvious in light of, the proposed combination of Fling, Mehta, Lee and Dingwall. Consequently, the rejection of these claims under 35 U.S.C. 103(a) should be withdrawn.

2. Claim 27 is patentable.

The Office Action incorrectly maintains a rejection of claim 27 as obvious over Yamashita (U.S. Patent No. 5,890,432) in view of Dingwall et al. (U.S. Patent No. 5,332,997).

The Office Action states that Yamashita shows (citing FIG. 4) a handset that includes a digital to analog converter 307, and that Dingwall discloses a switched capacitor DAC network

comprising a plurality of DACs 11 (citing FIG. 6) each of which comprises a plurality of capacitors that share charge with one another (citing FIG. 2).

The Office Action further states that Yamashita does not show a switched capacitor network having a plurality of DACs as recited in claim 27, but that it would have been obvious to utilize the switched capacitor DAC network in FIGS. 2, 6 of Dingwall for the DAC 307 in FIG. 4 of Yamashita, for the purpose of loading data at a high speed (citing col. 3, lines 29-35 of Dingwall et al., "for the purpose of loading data at a high speed").

1. The proposed combination is improper.

As previously explained **and not disputed in any way by the Examiner,** and as further discussed below, the proposed combination is improper for at least the following reasons: (1) the references teach away from the proposed combination, (2) the proposed combination would leave the circuit of Yamashita inoperative, and (3) even if the proposed combination would be operational, the Office Action has not presented legally sufficient evidence to support the proposed motivation, which is in fact illusory.

Yamashita discloses a handset in which speech signals are received from a microphone 106, coded by a speech CODEC 304 and a channel CODEC 305, and then modulated by a MODEM 306 to produces modulated in-phase (I) and quadrature-phase (Q) transmitting signals. A DAC 307 converts the modulated in-phase (I) and quadrature-phase (Q) transmitting signals to analog transmitting signals TxDI and TxDQ, respectively, that are transferred to the RF transmitter 202 of the system. (Column 5, lines 34-40).

Dingwall discloses (in FIG. 6), a serial data generator with 40 output data word lines (DWL1 through DWL40). Each output data word line carries 144 bits of serial information which are distributed onto 24 sublines. Each subline carries 6 digital data bits to a corresponding serial-input, binary weighted DAC 11, which converts the 6 serial data bits into an analog signal (col. 5, lines 5-15). The DAC 11 uses a binary weighted capacitive network 50, which is comprised of binary-weighted storage capacitors (FIG. 2, col. 5, lines 58-65).

First, observe that Dingwall itself **teaches away** from the proposed combination. Dingwall states that there are "*problems*" with the DAC shown in FIGS. 2, 6 (see col. 12, lines 15-22). Dingwall states that the binary weighted capacitive network used in the DAC of FIGS. 2, 6 and shown in FIG. 2, requires "*very large*" or "*very small*" capacitors (col. 12, lines 15-22)

(emphasis added). The very small capacitors are "*difficult to make accurately*" and there is the "*additional problem*" of stray capacitance (col. 12, lines 22-24) (emphasis added). On the other hand, large capacitors take "*too much space*" (col. 12, lines 23-25) (emphasis added). The "*problem becomes worse*" when more than 6 binary steps are desired (col. 12, lines 21-22) (emphasis added). Dingwall suggests that the problems "may be alleviated" by adding additional circuitry; however, in view of all of these problems, why would anyone skilled in the art even consider using the DAC of Dingwall in the handset of Yamashita? He all but expressly says not to! The Office Action fails to address this highly persuasive point, as previously noted. Instead, it relies on a speculative hindsight effort to pick and choose the features and qualities of the references to be combined. This is improper.

Second, the proposed combination would leave the circuit in Yamashita *inoperative*. The DAC 11 in Dingwall is a serial-input DAC. In contrast thereto, the DAC 307 of Yamashita is coupled to a channel coder 305 (which typically produce a parallel output), therefore suggesting that it is a parallel-input DAC (extra circuitry would be needed if the DAC 307 were not a parallel-input DAC). A serial-input DAC is not interchangeable with a parallel-input DAC, and therefore, cannot be substituted for the parallel-input DAC 307 of Yamashita, without leaving the circuit inoperative, a result that clearly makes the proposed combination improper. MPEP 2143.01 states that the proposed modification cannot render the prior art unsatisfactory for its intended purpose. Further, even if the circuit of Yamashita could be further modified (by adding additional circuitry not proposed by the Office Action) so as to operate with the DAC of Dingwall, such modifications have not been proposed by the Office Action, and the potential impact to size, cost, power, performance, etc., clearly teaches away from any attempts to do so.

The Office Action states that one skilled in the art would carry out the proposed modification for the purpose of loading data at a high speed (citing col. 3, lines 29-35 of Dingwall et al.). This proposed motivation is *illusory* and is an improper effort to find motivation where there is none. *Firstly, one skilled in the art would not make a modification that would leave the circuit unusable for its intended purpose*! Secondly, even if the proposed combination were operational, the Office Action has not presented legally sufficient evidence to support the proposed motivation.

To try to satisfy the Office's burden of proof as to motivation, the Office Action cites a statement from Dingwall to the effect that data is loaded very quickly onto the gates of the

switching transistors. The Office Action thus implies that one skilled in the art would make the modification to improve speed. However, the "evidence" set forth by the Office Action merely implies that the DAC in Dingwall may be faster than other *Dingwall-type* DACs. This says absolutely *nothing* about whether there is a speed advantage to putting the DAC of Dingwall into Yamashita, and is thus factually, logically and legally *irrelevant*. If speed is the concern, then the issue is not whether the DAC of Dingwall is faster than other Dingwall type DACs, but rather, the speed of the serial-input DAC in Dingwall compared to the speed of the parallel-input DAC in Yamashita. Yet the evidence set forth by the Office Action does not say anything about the speed of the DAC in Dingwall versus the DAC in Yamashita. Consequently, *there is no support for the contention that the proposed combination, even if operational, would be expected to produce a speed improvement in Yamashita.* Thus, the Office's burden of proof as to motivation is not met.

Moreover, because the DAC of Dingwall is a serial-input DAC and the DAC in Yamashita would appear to be a parallel-input DAC, it is likely that the DAC of Dingwall is actually *slower*, not faster, than the DAC in Yamashita, thereby actually teaching *away* from the proposed combination.

Consequently, the proposed combination is improper and neither Yamashita, nor Dingwall nor any legally tenable combination thereof, teaches or suggests the inventions recited in claim 27.

F. Rejections Under 35 U.S.C. §102

Paragraph 8 of the Office Action rejects claims 17-24, 28-33 and 38-40 under 35 U.S.C. §102(e) as being anticipated by Watson et al., 6,154,162. (Applicants wish to point out that there is no claim 28 pending in this application, and that there is also a claim 41 which has not been addressed but which depends from rejected claim 29; Applicants assume herein that the rejection is of claims 17-24, 29-33, and 38-41.) Applicants respectfully traverse this rejection.

1. Prima Facie Insufficiency of the Rejection

This rejection, unfortunately, is insufficient on its face, to a degree that the Action should be withdrawn and a new one issued. Among the rejected claims there are at least *three dozen* elements and limitations. The exposition of the rejection in paragraph 8 is less than three lines

long, identifying in Watson only scrambler 42, SC DAC 32, capacitors 70, 72, and 74, and an unsupported assertion that the capacitors share charge. Applicants are left to speculate where the Examiner believed he may have found all of the *other* claim elements and limitations. Both under 37 C.F.R. 1.104(c)(2) and the corresponding MPEP mandate to explain the rejection in sufficient detail to permit consideration and response by Applicants, this rejection fails to meet the requirements. Accordingly, no response is required.

Nevertheless, to advance prosecution, Applicants will distinguish Watson.

2. Discussion of Watson

Watson is directed to a digital-to-analog converter (DAC) which uses switched capacitors summed to an op amp to generate an analog voltage (Abstract). Watson makes use of a thermometer encoder to reduce the size of capacitors used, and thus reduce the error in the capacitor (col. 4, lines 20-32). Watson makes use of a scrambler to further reduce the dependency of the error on a select few of the capacitors (col. 4, lines39-50). Only the higher order bits are scrambled in order to reduce complexity and cost (col. 4, lines 51-56).

3. Applicants' Claims Distinguish Over Watson

The Office Action states in its rejection that Watson discloses in Fig. 4 a digital signal processing system comprising: scrambler 42, switched capacitor DAC 32 including a plurality of capacitors 70, 72, and 74 *sharing charge with one another*. Applicants respectfully disagree. The Examiner has misunderstood Watson. Claim 17 is directed to "a system having a digital signal processing stage comprising a scrambler that receives a multi-bit input and provides a multi-bit output; and a switched capacitor DAC that receives a multi-bit input signal that includes the multi-bit output of the digital signal processing stage, the switched capacitor DAC having a plurality of sub DACs that each receive an associated amount of charge in response to the multi-bit input signal received by the DAC, the switched capacitor DAC *having an operating state in which at least two of the plurality of sub DACs share charge with one another such that the associated charges are redistributed*, and having an operating state in which the switched capacitor DAC outputs an analog signal that is indicative of the multi-bit input signal received by the switched capacitor DAC using less than all of the redistributed charge."

Quite simply, nowhere does Watson disclose a device in which at least two of the plurality of subDACs share charge with one another such that the associated charges are redistributed (i.e., between capacitors).

Referring to Fig. 4 of Watson, each of the capacitors 70, 72, and 74 referenced by the Office Action correspond to the subDACs of claim 17. However, these capacitors are connected through a node which is forced to maintain a specific voltage. Watson discloses that when switches 78 are connecting capacitors 70, 72, and 74 to Vref or ground, switch 68 connects node 58 to a constant voltage VCM (col. 6, lines 43-45). Watson states, "Thus, both sides of capacitors 70, 72, 74, and linking capacitor 50 are driven to constant voltages, allowing the capacitors to be fully charged or discharged." (col. 6, lines 45-48). **Since both terminals of every subDAC capacitor of Watson are driven to a constant voltage, there can be no charge sharing of charge with one another such the associated charges are redistributed.** This is almost as explicit a teaching away from the claimed invention as one could imagine finding.

Watson does disclose that in the summing phase of operation, the charge of the subDAC capacitors 70, 72, and 74 is discharged from the summing node 58 into the bypass capacitor 60 (col. 6, lines 52-60). However, this does not constitute charge sharing between the subDAC capacitors, since the charge on any subDAC capacitor 70, 72, or 74 cannot affect the charge on any other capacitor.

For at least the foregoing reasons, claim 17 distinguishes over Watson, and the rejection of claim 17 under 35 U.S.C. §102(e) as being anticipated by Watson must be withdrawn.

Claims 18-21 depend from and further limit claim 17, and are believed to be allowable based on their dependency.

Claim 29 likewise recites, inter alia, "the switched capacitor DAC **having an operating state in which at least two of the plurality of sub DACs share charge with one another such that the associated charges are redistributed.**"

For the same reasons discussed above in connection with claim 17, therefore, claim 29 patentably distinguishes over Watson.

Claims 32 and 39-41 depend from claim 29, and are believed to be allowable based on their dependency.

Claim 22 is directed to a digital-to-analog converter that receives a multi-bit digital signal and produces an analog output that is **proportional to the square of the multi-bit digital signal**.

The Office Action has failed to specifically address the limitations of claim 22 with respect to the rejection under 35 U.S.C. §102(e), instead choosing to blindly group it with claim 17, which is not at all similar. Nonetheless, as is obvious, nowhere does Watson disclose a DAC that receives a multi-bit digital signal and produces an analog output that is **proportional to the square of the multi-bit digital signal**.

Therefore, claim 22 patentably also distinguishes over Watson, and its rejection must be withdrawn.

Claims 23-24 depend from claim 22, and are allowable for at least the same reasons.

Claim 33 is directed to a system comprising: a digital signal processing stage that receives a multi-bit input and provides a multi-bit output; and a switched capacitor DAC wherein the DAC comprises a switched capacitor network that receives a multi-bit input that includes the multi-bit output from the digital signal processing stage, the switched capacitor network having a plurality of sub DACs that each receive an associated bit of the multi-bit digital signal, each of the plurality of sub DACs having an associated capacitance that receives an associated amount of charge in response to the associated bit, **the DAC having an operating state in which at least two of the plurality of sub DACs share charge with one another**, and having an operating state in which less than all of the plurality of sub DACs are connected to an output terminal and the switched capacitor network outputs at least one analog signal indicative of a sum of values of bits in the multi-bit input received by the DAC.

For at least the reasons discussed above in connection with claims 17 and 29, claim 33 patentably distinguishes over Watson. Namely, nowhere does Watson teach or disclose a DAC having an operating state in which at least two of the plurality of sub DACs share charge with one another. Therefore, the rejection of claim 33 as being anticipated by Watson should be withdrawn.

Claim 34 depends from claim 33, and is allowable for at least the same reasons.

Claim 38 was rejected under 35 U.S.C. §102(e) over Watson; however, claim 38 depends from claim 1, which has been rejected under 35 U.S.C. §103 in the same Office Action. Since claim 1 is believed to have been placed in condition for allowance previously in this response

and has not been rejected under 35 U.S.C. §102(e) over Watson, Applicants do not address the rejection of claim 38, as it is believed to be allowable based on its dependency. However, Applicants reserve the right to make such an argument in the future.

G. Provisional Double Patenting Rejection

Paragraph 10 of the Office Action states that claims 1-9 and 34-37 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting over claims 1-17 of copending Applicant No. 09/575,561.

Applicants note that these rejections are provisional and therefore do not require a response at this time. However, Applicants expressly reserve the right to respond at a future time.

CONCLUSION

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicants' attorney at the telephone number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicants hereby request any necessary extension of time. If there is a fee occasioned by this response, including an extension fee that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,

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Docket No.: A0312.70409.US
Date: December 20, 2002

x12/20/02

Marked-Up Specification

Please replace the paragraph beginning on line 24 of page 9 with the rewritten paragraph shown below:

--FIG. 1 is a block diagram of one embodiment of a portion of a handset 50 for a mobile communication system. The handset 50 includes an input portion having a transducer 54 that receives an input signal 56, e.g., a voice or other acoustical signal, representing information to be communicated via the mobile communication system. The transducer 54 converts the input signal 56 into an electrical signal, typically an analog signal, which is supplied to an analog-to-digital converter (ADC) 58, for example a voice band ADC. The ADC 58 periodically samples the electrical signal and generates a sequence of multi-bit digital signals, which are supplied to a digital baseband processor 60. The baseband processor 60 performs further signal processing, including for example, compression. The output of the baseband processor 60 is supplied to burst store stage 62, which feeds a GMSK modulator 64. The GMSK modulator 64 produces multi-bit digital signals, which is supplied via signal lines, represented by a signal line 66, to a digital to analog conversion system 68. The digital to analog conversion system 68 converts the sequence of multi-bit digital signals into an analog signal, which is supplied via signal line 70 to an output portion 72. The output portion 72 includes a mixer [72] 74 that receives the analog signal on signal line 70 and feeds a transmitter 76, which in turn transmits the signal. DAC can be used in any digital to analog conversion.--

Please replace the paragraph beginning on line 16 of page 20 with the rewritten paragraph shown below:

--FIG. 15 is a block diagram of another embodiment of the SC DAC 150, which is similar to the SC DAC 150 illustrated in FIGS. 9, 10A-10C, except that the SC DAC 150 of FIG. 15 further comprises a switch [148] S48, a switch [149] S49, and a switch [150] S50. A first terminal of the switch S48 is connected to the second terminal of the charge sharing switch S43. A first terminal of the switch S49 is connected to the second terminal of the charge sharing switch S45. A first terminal of the switch S50 is connected to the second terminal of the charge sharing switch S46. Each of the switches S48, S49, and S50 may, but need not serve one or more of the functions noted hereinbelow. In one embodiment, one purpose of the switches S48,

S49, S50 is to provide parasitic capacitance similar to that of output switch S47, so as to help cancel the effect of the parasitic capacitance of switch S47.--

Please replace the paragraph beginning at line 16 of page 20 with the following rewritten paragraph:

--FIG. 15 is a block diagram of another embodiment of the SC DAC 150, which is similar to the SC DAC 150 illustrated in FIGS. 9, 10A-10C, except that the SC DAC 150 of FIG. 15 further comprises a switch [148] S48, a switch [149] S49, and a switch [150] S50. A first terminal of the switch S48 is connected to the second terminal of the charge sharing switch S43. A first terminal of the switch S49 is connected to the second terminal of the charge sharing switch S45. A first terminal of the switch S50 is connected to the second terminal of the charge sharing switch S46. Each of the switches S48, S49, and S50 may, but need not serve one or more of the functions noted hereinbelow. In one embodiment, one purpose of the switches S48, S49, S50 is to provide parasitic capacitance similar to that of output switch S47, so as to help cancel the effect of the parasitic capacitance of switch S47.--

Please replace the paragraph beginning at line 27 of page 13 with the following rewritten paragraph:

--The DAC 150 may receive a non-overlapping 3-phase clock, P1, P2, P3, shown in FIG. [3] 6. The closed/open condition of the switches S3, S6, S9, and S12 is controlled by the P3 signal of the 3-phase clock. The P1 signal of the 3-phase clock controls the open/closed condition of the charge sharing switches S13, S14, S15, and S16. The P2 signal of the 3-phase clock controls the open/closed condition of the switch S17.--